MCS 920B TECHNICAL MANUAL

CATALOGUE NO. MCB 143

PART 5: OPERATIONAL/TEST EQUIPMENT

CHAPTER 1: INTRODUCTION

CHAPTER 1

CONTROL UNIT

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CHAPTER 1

INTRODUCTION

1. GENERAL

The MCS 920B Computer is designed to function either under manual control, by means of a control unit, or automatically (when a program is loaded) by means of a start address plug.

An alternative method of use is available employing a program loading unit. This allows a start address plug to be substituted to run the computer when the program has been read in. Details are given in Pt. 5, Chap. 5.

Diagnostic testing is carried out by means of test programs listed in the 920B Test Program Library (Cat. No. MCB 145). Such tests are run from the control unit and results are generally output via the tape punch.

Visual indication of computer registers and control bistables is provided by the display unit (Pt. 5, Chap. 3) which, when used with a control unit, allows the engineer to verify computer operation and fault find. Such testing can include:

(i)   the obeying of stored instructions

(ii)   entering and obeying an instruction set on the number generator keys

(iii)   the 'single-shot' technique in which each step of the micro-program for a chosen instruction is available for display and examination

2. TESTING

When the 'single-shot' technique is to be employed, the engineer should consult Figs. A11 and A12 (the Control Sequence) which detail the micro-

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instructions for each function. With both control and display units connected to the computer (and the former placed in the TEST MODE), the engineer can set up an instruction which failed. Using the procedure given below and comparing displayed information with the Control Sequence the area of fault can be determined. Where, for example, a fault occurs in one bit position of a register, Fig. A3 (which details the computer logic boards, their functions and positions) enables ready identification of the affected board.

Whilst the function of each control is described in Pt. 5, Chap. 2 the following procedures for the use of the control unit in the test role is designed to familiarise the engineer with its method of operation. Since a display unit is fundamental in maintenance, this unit must be connected to the computer before any testing is attempted.

NOTE: The computer must be switched off before connecting the display unit.

The control unit MODE switch must be placed in the TEST position.

NOTE: The Yale-type key operating this switch cannot be removed whilst TEST is selected, and serves as a reminder that all controls are effective.

When formulating an instruction to test the computer and not making use of stored information, the two necessary operands must first be entered, e.g. addend and augend, multiplier and multiplicand, etc.

The first operand is set on the word generator keys, and ENTER raised (this position gives 'single enter'). This action places the operand in the A-register (confirmed by the display). ENTER should be returned to NORMAL at this time. A write instruction is required to place this operand into a store location, this is accomplished by setting 5 on the function keys, a specified address on the N keys, and raising OBEY. (Return OBEY to NORMAL on completion).

The second operand may now be entered into the A-register, using the first part of the above procedure. The instruction is obeyed by setting the required function on the F keys, the address of the appropriate store location on the N keys and raising OBEY (all other engineers switches must be in the off position). The result is placed in the A-register and displayed. OBEY should be returned to NORMAL.

Assuming stored information is to be verified, read desired location and compare against the program sheets. Alternatively a write instruction followed by a read will confirm store circuits are functioning correctly.

To verify a particular instruction, comparing the micro-instructions with the Control Sequence, 'single-shotting' may be carried out as follows:

(i)   Enter the appropriate operands   or

(ii)   Read an appropriate operand from a stored program to set the A-register (this will be displayed).

(iii)   Set the N-keys to the address of the location holding the second operand, the F-keys to the function to be obeyed. Select CYCLE STOP and depress RESTART

This initiates the first block of micro-instructions for the function. The selected function number is set on the I-register neons and register contents are displayed on the neons of the appropriate registers. The binary address of the micro-program matrix appearing on the display unit neons designated THIS CYCLE indicates the micro-instruction block to be performed when RESTART is next pressed. These micro instructions may, however, be modified by the CONDITIONALS governing the choice of micro-instruction blocks. These are detailed by the Control Sequence. NEXT CYCLE neons display the matrix address of the succeeding micro-instruction block.

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The computer stops at this junction, proceeding to the next micro-instruction block when RESTART is pressed.

The function is completed when the final result appears in the A-register after pressing RESTART the appropriate number of times to progress around the Control Sequence of the chosen function.

Continuous repetition of any step of the micro program is achieved by selecting CYCLE REPEAT and pressing RESTART.

When oscilloscope-testing a logic board, the appropriate waveforms can be monitored by using the continuous OBEY or continuous ENTER facility (i. e. depressing these switches).

To check that an instruction is obeyed correctly, e. g. by comparing the displayed result with a worked example or punching a character from the A-register on to paper tape, etc. , the ORDER STOP facility can be used. This enables an instruction set on the word generator to be obeyed in one step by selecting ORDER STOP and depressing RESTART.

Full details of the micro program, together with worked examples of the functions, are given in Pt. 1, Chap. 4 of this Manual.

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CHAPTER 2: CONTROL UNIT, MCB. 40, 41.

CHAPTER 2.

CONTROL UNIT.

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          (Issue 1)

LIST OF FIGURES

1.   INTRODUCTION

The Control Unit.

Its use permits operation of the computer independently of its peripheral system, enabling engineering tests to be carried out.   It is also used as an operational control panel.   The layout of the Control Unit is given in Fig. a.

1.1.   Control Switches.

The control switches of the Control Unit (Fig. A22) are grouped on the front panel in the following manner:

S1   COMPUTER MODE SWITCH AND MASTER CONTROL

MODE 1   AUTO

MODE 2   OPERATE

MODE 3   TEST

S2   JUMP

S3   STOP   Red illuminated

S4   RESTART

S5   RESET   Amber Illuminated

S6   ON   Green Illuminated

S7   OFF   Red Illuminated

S8   OBEY

S9   ENTER

S10 CYCLE STOP-ORDER STOP

S11 CYCLE REPEAT

S12 INTERRUPT   1

S13 LEVER   1   TRACE, AUTO, MANUAL

S14   INTERRUPT   2

S15   LEVEL   2   TRACE, AUTO, MANUAL

S16   INTERRUPT   3

S17   LEVEL   3   TRACE, AUTO, MANUAL

S18-S30   N-ADDRESS   )
S31-S34   F-FUNCTION   )   WORD GENERATOR
S35   B-MODIFICATION   )

INTERRUPT LAMP LEVELS.

1LP 12A   INTERRUPT 1   Red illuminated

1LP 12C   LEVEL   1 (Active 1)   Green illuminated

1LP 14A   INTERRUPT 2   Red illuminated

1LP 14C   LEVEL   2 (Active 2)   Green illuminated

1LP 16A   INTERRUPT 3   Red illuminated

1LP 16C   LEVEL   3 (Active 3)   Green illuminated

2.   The Computer Mode Switch Positions.

The computer mode switch is a three position security switch which enables the control panel to be locked in the required mode of operation.

2.1.   MODE 1: AUTO

When the AUTO Mode is entered the '0' volt rail is disconnected from the JUMP S2 Circuit and the Number Generator Keys. Together with the Auto signal this enables the computer to set the Wn inputs of the M-register to

8 8177. This corresponds to Function 8, The Jump instruction, and enables the computer to place the Program Trigger Address (8177) into the Sequence Control Register when the J1A signal is generated in the computer. (Figs. A15 and A13 refer).

The circuit configuration of the mode switch is such that in the AUTO mode manual interrupt of the computer is inhibited.

It must be noted that the program interrupt facility and trace facility remain unaffected.

NOTE: The Control Unit does not turn power ON or OFF automatically when AUTO is selected. The jump to program trigger location 8177 occurs when the ON button is pressed.

This system differs from AUTO operation when using a Program Loading Unit (MCB 62) or Start Address Plug (MCB 42) by the absence of Autostart Links across computer SKT 11 pins $\underline{r}$ and $\underline{s}$ which maintain the start signal to the computer power supply unit, (Fig. b refers).

Fig. b also shows the conditions between Control Unit PL. 2 and computer SKT 11 to obtain the automatic jump instruction. In binary form this is

$$0 \quad 1000 \quad 111111110001$$

or $\overline{\text{NG 18}}$, NG 17, $\overline{\text{NG 16}}$, $\overline{\text{NG 15}}$, $\overline{\text{NG 14}}$, NG 13, NG 12, NG 11, NG 10, NG 9, NG 8, NG 7, NG 6, NG 5, $\overline{\text{NG 4}}$, $\overline{\text{NG 3}}$, $\overline{\text{NG 2}}$ and NG 1 respectively.

These connections are open circuit at the Control Unit when AUTO mode is selected (Fig. A. 22 refers). However, the bar waveforms are inverted by LSA 18s (A-FS boards) to set '0's in the M-Register whilst 'AND' gating with WTM sets the waveforms NG 1, NG 5, NG 6 etc. directly into the M-Register (Fig. A. 13 refers).

2.2 Mode 2: OPERATE

Control Unit switches associated with OPERATE and TEST Modes are held open-circuit via the MODE switch until the appropriate mode of operation is selected.

The armatures of these switches are then returned to OV, thus permitting the switch to become effective by placing a logic '0' (when operated) at the LSAs of the Manual Control logic of the central processor (Fig. A. 15 refers).

NOTE: LSA 18s (single input noise rejection invertors) are used which give a logic '0' output 1 millisecond after the input goes to logic '1'. This delay nullifies the effect of switch contact-bounce.

When switched to the OPERATE mode, the computer mode switch permits the jump instruction to be initiated on the operation of the JUMP switch which sets NG 17 to open circuit and NG 17 to 0 volts. The computer then jumps to the location addressed by the number generator keys.

The following additional controls are effective:

1. Address generator keys

2. Jump, Restart and Stop

3. Program Level Controls

These controls make sufficient functions available for reading new programs and for the checking of programs using the TRACE facility.

2.3 Mode 3: TEST

When switched to the TEST mode all controls become available. These are used by the engineer when locating faults. This mode is normally used in conjunction with the Display Unit, MCB 43, 44 selecting either OPERATE or TEST modes, to enable the manual interrupt push buttons on the Honeywell single shot units to produce a positive

going pulse of 6 volts with respect to 0V by setting the appropriate PROGRAM LEVEL switch to MANUAL.

3.   Group S2 JUMP, S3 STOP, S4 RESTART

3.1 S2 JUMP

Operation of this switch will initiate a jump instruction to the address set-up on the number generator keys. The computer may be stopped or running during this operation.

3.2 S3 STOP

This is a red illuminated push button switch. When operated it will stop the computer at the end of the current instruction. The lamp driver LD1 is energised, lighting the indicator lamp ILP3 when the computer is in the STOP state. The STOP condition can only be terminated by operation of the RESTART or JUMP controls.

3.3 S4 RESTART

This is a push-button switch, when operated, it will restart the computer if it has previously been stopped and is not in reset. This control is ineffective when the computer is in AUTO. When in the TEST mode, the CYCLE STOP and ORDER STOP controls modify the effect of this control. Operation will then initiate one cycle or one instruction.

4.   Group S5 RESET, S6 ON, S7 OFF

4.1 S5 RESET

The RESET control is an amber illuminated push-button switch that lights-up when the indicator lamp ILP5 is energised by lamp driver LD2 when the computer is in the RESET state. Operation of this switch returns the computer to the reset state. This state is also caused by the switch-on sequence. The RESET state can only be terminated by a

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Jump function, generated either automatically by the switch-on sequence in AUTO or by operation of the JUMP control or by operation of ENG and ONG switches whilst computer is in STOP mode. The RESET condition cannot be terminated if the power supplies are incorrect, or if the store is outside its operating temperature range.

4.2 S6 ON

Power ON is a green illuminated push-button switch. Operation of this control will initiate an up-sequence of power. The indicator lamp ILP6 will be illuminated when power is applied to the computer. The power on up-sequence also sets the computer to the RESET state. When in the AUTO mode, it initiates a jump function to location 8177 thus triggering the program.

4.3 S7 OFF

When the Power OFF switch is operated, it will initiate a down sequence of power to the computer to ensure that the contents of the store are not corrupted. The indicator lamp ILP7 will be illuminated red if the prime power supply is available, but the stabilised power unit is switched off.

5. Group S8 OBEY, S9 ENTER, S10 CYCLE-STOP, ORDER STOP
S11 CYCLE REPEAT.

5.1 S8 OBEY NUMBER GENERATOR

The OBEY NUMBER GENERATOR switch SW8 is a three position switch designated: CONTINUOUS, NORMAL and SINGLE SHOT. It determines if instructions are accepted from the Number Generator or store. When the OBEY NUMBER GENERATOR Key S8 is operated, the computer will obey the instruction set-up on the number generator keys. This control is only effective in the TEST mode and if the computer is stopped. In the NORMAL position, the number generator is not obeyed.

5.2 S9 ENTER NUMBER GENERATOR

The control is a three position switch, SINGLE SHOT, NORMAL and CONTINUOUS. In the up position the number is entered in a Single Shot mode, in the down position the number is entered continuously.

The operation of this switch allows the word set-up on the 18 key switches to be placed in the A register of the computer in the Continuous and Single Shot positions. This control is only effective in the TEST mode and if the computer is stopped. In the NORMAL position, the Number Generator is not entered.

5.3 S10 STOP MODE

This control is a three position switch with positions CYCLE STOP, NORMAL and ORDER STOP and is only effective in the TEST mode. In the " up " position the computer is set in the CYCLE-STOP mode, in which the computer obeys successive steps in the micro-program each time the RESTART switch is operated.

In the " down " position, the computer is set to the ORDER-STOP state in which it will obey a stored program one instruction at a time. Each successive order is initiated by operation of the RESTART control.

5.4 S11 CYCLE REPEAT

This key-switch is only effective in the TEST mode. When it is set to the up position the computer repeats a micro-step. Repetition will occur each time RESTART is operated when CYCLE STOP is also set, or if CYCLE STOP is not set, repetition will occur continuously.

6. <u>INTERRUPT, LEVEL, TRACE/AUTO/MANUAL.</u>

Group S12 INTERRUPT 1.	TRACE/AUTO/MANUAL
Group S13 LEVEL 1.	TRACE/AUTO/MANUAL
Group S14 INTERRUPT 2.	TRACE/AUTO/MANUAL
Group S15 LEVEL 2.	TRACE/AUTO/MANUAL
Group S16 INTERRUPT 3.	TRACE/AUTO/MANUAL
Group S17 LEVEL 3.	TRACE/AUTO/MANUAL

These controls occur in two groups on the panel. They comprise three push-button illuminated switches and three key switches. Both a single push-button switch and a key switch is associated with each of the program levels 1, 2 and 3.

Each indicator is divided into two parts, the upper part is illuminated red when an interrupt condition has been received, and the lower half illuminated green when the corresponding program level is being obeyed.

The inputs ACTIVE 1, ACTIVE 2 or ACTIVE 3 switch-on the lamp drivers LD4, LD6 or LD8, (when the input goes to logic '0') lighting lamps ILP12C, ILP14C, or ILP16C.

When the key switches are in the down position, the associated level is set to MANUAL and external interrupt signals will be ineffective. When set to the " up " position, a permanent interrupt condition is generated for use with the TRACE program, with the armature of switches S13, S15 or S17 taken to +6V.

The push buttons are only effective when the corresponding level is set to MANUAL. In this case operation of the push button will generate an interrupt condition by means of the Honeywell single-shot units which are switched into the circuit when the Level switch is in MANUAL, the return line being made to 0V via switches S13, S15 or S17 (pin 6). Under this condition $\overline{PS\ 1}$, $\overline{PS\ 2}$ or $\overline{PS\ 3}$

becomes logic '0' to suppress peripheral interrupts.

7. NUMBER GENERATOR

Group S18-S30	N-ADDRESS WORD GENERATOR
Group S31-S34	F-FUNCTION - WORD GENERATOR
Group S35	B-MODIFICATION - WORD GENERATOR

The number generator comprises 18-key switches corresponding to the 18 bit positions in the computer word. Operating any key specifies a one in the corresponding bit position of the word.

The number generator is used for the following three purposes:

7.1 Address for JUMP operation

In this case only the less significant 13 bits of the number generator are effective and they specify the address of the JUMP function.

7.2 Number to be entered in the accumulator

All 18 bits specified by the keys are copied into the accumulator when the ENTER control is operated.

7.3 Instruction

Instruction to be obeyed when the OBEY control is operated.

8. AURAL MONITORING

The audio unit provides aural indication that a program is running. The circuit includes a diode/transistor NAND gate D1 (D2, D3) and VT3, transistor switch VT4, unijunction relaxation oscillator VT5, C2 and amplifier VT6.

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Audio tone is dependent upon the repetition frequency of waveform VTG (the collate waveform of the central processor) which operates transistor switch VT4 via a NAND element formed by D1 (D2, D3) VT3.

VT4 produces a ramp voltage at the input of unijunction relaxation oscillator VT5 by charging and discharging C2 in sympathy with VTG.

Audio output from oscillator VT5 is developed across VT6 and RV1, the latter setting the output level.

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CHAPTER 3: DISPLAY UNIT (MCB 43, 44)

CHAPTER 3

DISPLAY UNIT (MCB 43, 44)

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(Issue 1)

display unit

DISPLAY UNIT, 19" RACK MOUNTING
STANDARD VERSION

(CAT. Nº MCB 43)

FIG. C.

CHAPTER 3

THE DISPLAY UNIT MCB 43 AND 44

1. INTRODUCTION

The Display Unit is used in conjunction with the Control Unit when tests are carried for locating faults in the computer.

The Display Unit is provided with neon indicators which display the state of the computer registers and some control bistables.

A circuit diagram of the Display Unit is given in Fig. E1.

2. THE DISPLAY UNIT

2.1 Mechanical (MCB 43 and MCB 44)

The Display Unit is available in two versions, MCB 43 is for 19" rack mounting and MCB 44 a free standing unit.

2.2 Power Supply

The Display Unit is connected to the +6V d.c. and -6V d.c. supplies of the computer. The unit contains an inverter which converts the voltage received from the computer into the voltage needed to operate the unit.

2.3 Interconnections

The Display Unit is connected to the computer by three-61-way cables ten feet in length. This is shown in the drawing Fig. A1.

3. THE CIRCUIT OF THE DISPLAY UNIT

The circuit of the Display Unit consists of two separate units.

(a) The Power Supply

(b) The Indicating Unit

(Issue 2)

3.1 The Power Supply

The power supply of the display unit consists of an inverter and a rectifier circuit. The schematic diagram of the unit is given in Fig. E1.

3.1.1 The Inverter

The Inverter is of the free running type consisting of the transformer T1, transistors VT1, VT2 and diodes D1 and D2. VT1 and VT2 with the associated circuit components comprise a free running inverter whose frequency is controlled by the inductance of T1, giving an essentially square wave output at the secondaries of T1.

The source of the input +6V d.c, -6V d.c. is the computer power supply. The capacitor C5 across the input decouples the supply and prevents inverter noise from entering the supply. The capacitance of C5 is high because of the current demands of the inverter.

When power is first switched-on the network C2-R3 supplies a starting bias via the transformer to the bases of VT1 and VT2.

Due to initial unbalance either VT1 or VT2 will switch on. Assume VT1 switches on, VT2 will be switched off via the positive feedback from transformer T1. VT1 will remain on until the transformer tends to saturate due to the magnetising current; VT1 cannot be kept switched on as there is insufficient drive. The transistor switches off switching on VT2. The components R1, C1, D1 and D2 reduce voltage transients when the transistors switch off.

3.1.2 The Rectifier

The two secondaries of T1 are isolated from each other and have different output voltages. Both outputs are rectified by bridge rectifiers and smoothed to give +70V d.c, 0V, and -40V d.c.

3.2 The Indicating Unit (B-Q Unit)

There are 5 P.C. boards in this unit. Each is identical (for interchangeability) and contains 40 neon indicators and their associated drivers.

3.2.1 Neon Driver Circuit

Referring to circuit El the base of VT3 is connected to the bar output waveform via a 3.9K resistor in the computer. If the logic term to be displayed is at a logic '1', the bar waveform will be at logic '0' and VT3 will be switched off. The voltage across the neon is then 110V which strikes the neon.

The striking/burning voltage is in the range 90V to 65V. If VT3 is switched on the voltage across the neon is insufficient for it to remain on.

3.2.2 Display Waveforms

The lamps indicate the state of the following:

The A Register	1 to 18 (A)
The Q Register	1 to 18 (Q)
The G Register	1 to 18 (G)
The M Register	1 to 18 (M)
The J Register	1 to 16 (J)
The Process Counter	1 to 12 (PC)
Peripheral Address	1 to 11 (P)
Peripheral Select	1 lamp (STR) Select Tape Reader
"	1 lamp (STP) Select Tape Punch
"	1 lamp (SIP) Select Input
"	1 lamp (SOP) Select Output
The I Register	1 to 4 (I)
Microstage (Current Cycle)	1 to 3 (CS)

Microstage (Next Cycle)	1 to 3 (CCS)
Conditionals	1 to 3 (CA, CB, CD)
Control/Function	1 to 2 (CN, FD)
Not Ready	1 (NOT READY)
Store Temperature Low	1 (STL)
Reset	1 (RESET)
Stop	1 (STOP)
Overflow X bistable	1 (X)
Overflow Y bistable	1 (Y)

Full details of the control waveforms appear in Part 1, Chapter 4 of this Manual.

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PART 5: TEST EQUIPMENT

CHAPTER 4: THE MARGINAL TEST UNIT MCB 52

CHAPTER 4

THE MARGINAL TEST UNIT

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MARGINAL TEST UNIT
(CAT. Nº MCB 52)

FIG. d.

CHAPTER 4

MARGINAL TEST UNIT

1.   INTRODUCTION

The Marginal Test Unit is designed to check the operation of the computer by applying a series of marginal tests to it.

When conducted at regular intervals these tests will reveal the condition of the computer and indicate the corrective measures necessary to prevent possible failure. To accomplish some of these tests either an MCB 21 or MCB 24 power supply is used. When marginal tests are applied the functions are varied independently for each specified test. A drawing of the unit is shown in Fig. d.

1.1   The Margin Functions

The margin tests applied are as follows:

(a)   + 6V and - 6V margins with MCB 21 Power Supply

(b)   Inhibit variable supply with MCB 21 Power Supply

(c)   Drive Current from Master Drivers A-EC3 unit

(d)   Main Timing loop

(e)   Pulse width of pulse generator output

The indicating meter is switched into the circuit of each function by the meter switch. With the exception of the 6V margins test which has a three position switch, each test is switched into circuit by a margins ON/OFF switch. The level of margins applied is controlled by a potentiometer associated with each of the marginal functions.

2.   INTERCONNECTIONS

The Marginal Test Unit may be connected to the computer at socket 7 by a single 10 ft. multiway cable. This may be seen in the drawing

Fig. A1 (Pt. 1, Chap. 1, Sec. (v))

   Interconnections to the Additional 8192 word Store block is at socket 12. This is shown in Fig B4 (Pt. 2, Chap. 2, Sec. 2).
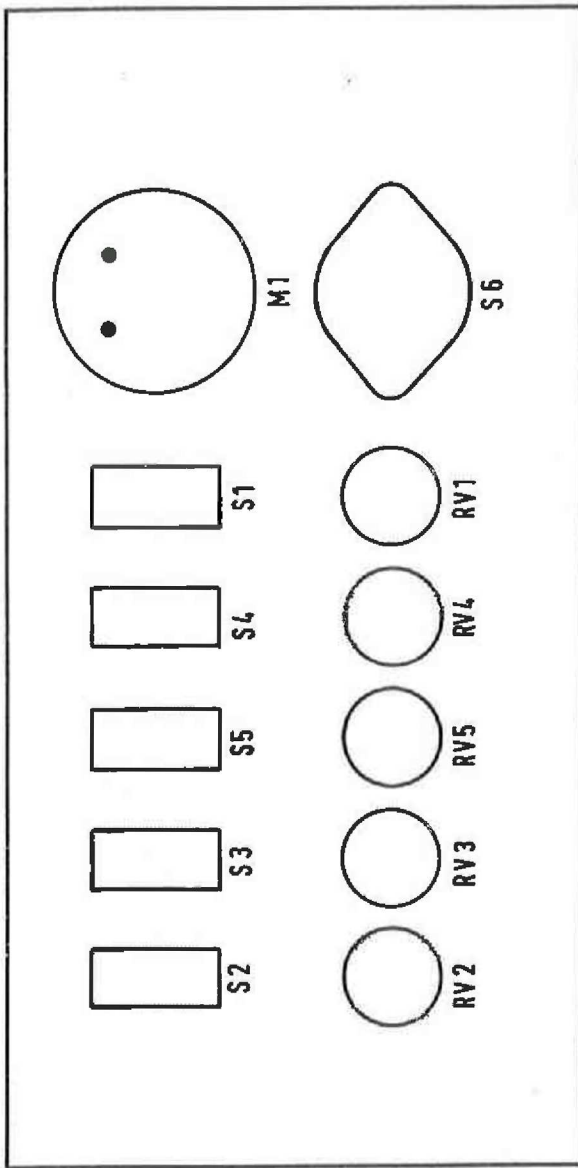
   Interconnections to the 16,384 words Store is at socket 12. This is shown by Fig. B1, Sht 2 (Pt. 2, Chap. 1, Sec. 4.3).
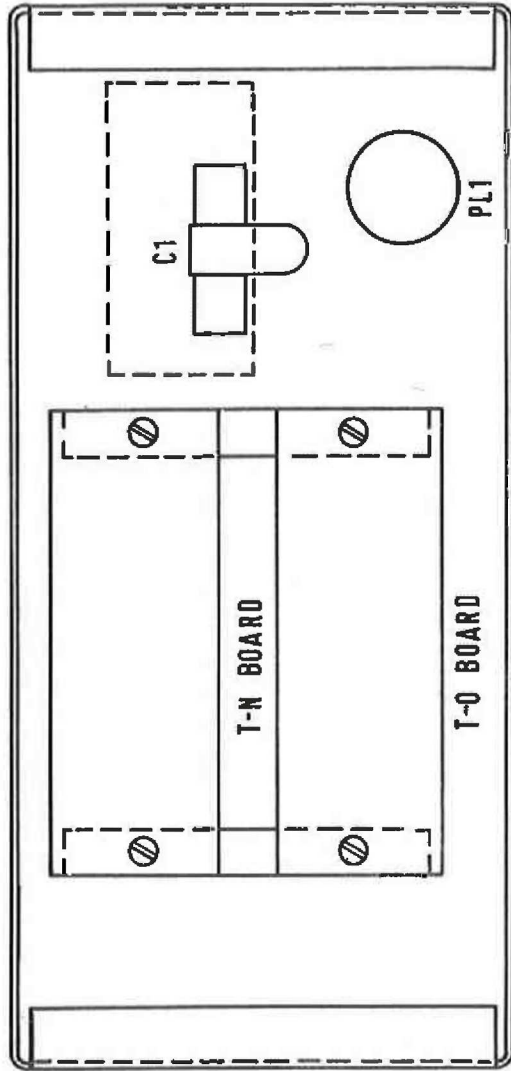
3. CONSTRUCTION

   The components of the Marginal Test Unit are mounted within an aluminium cabinet of the dimensions $12\frac{1}{2}$" wide x 7" deep x 7" high. The unit is equipped with rubber feet and weighs approximately $9\frac{1}{2}$ lbs.

   The meter, meter switch, margin function switches, potentiometers and two handles are mounted on the front panel which is attached to the cabinet by four screws.
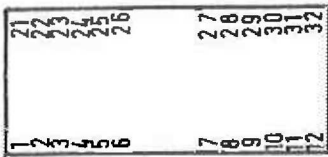
   The boards on which the electronic components are mounted are affixed to the rear panel by stand-offs. The plug for the test cable is also mounted on the rear panel. The component layout of the unit is given in Fig. e.
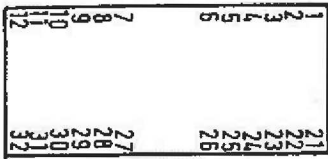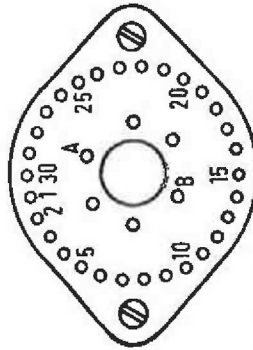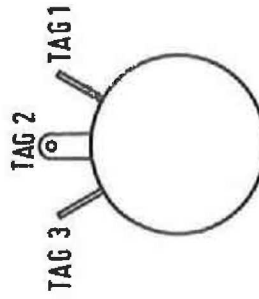
Typical view
On rear of S2,S3,S4,S5.

Typical view
On rear of S1

Typical view on rear of
2 pole rotary switch.

Typical view on rear of
variable resistors

TAG 1
TAG 2
TAG 3

M1

S6

S1

S4

S5

S3

S2

RV1

RV4

RV5

RV3

RV2

View on rear of front panel

C1

PL1

T-N BOARD

T-O BOARD

View on rear of chassis

Fig. e. Marginal Test Component Layout.

ISS. 1.

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Fig. f. T-N and T-O boards of the Marginal Test Unit

ISS. 1.

* Selected on Test

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4.   POWER SUPPLIES

The marginal test circuits are connected to modify the control lines of the circuits under test. The additional power required is very low and is derived from the circuits under test.

5.   THE CIRCUIT

The circuit diagram of the Marginal Test Unit is given in Fig. E2; it consists of (a) A meter switching circuit actuated by meter switch S6. (b) ON/OFF switches S1, S2, S3, S4 and S5 for each function. (c) Series current limiting resistors and (d) Potentiometers for each function.

Direct indication of positive and negative margins are given on a zero centre 250-0-250 micrometer. The resistors R3, R6, R9, R13 and R18 are adjusted so that a full scale deflection of 15% results when 15% margins are applied.

5.1   Circuit Boards

There are two circuit boards within the Marginal Test Unit, the T-O board and the T-N board as shown in Fig. f.

5.1.1   The T-O Board

The T-O board holds the current control resistors that are connected in series with the Function Test switches and potentiometers. The resistors for current control are connected in parallel and one is adjusted during manufacture to calibrate the meter.

5.1.2   The T-N Board

The resistors in series with the control potentiometer are mounted on the T-N board. They are directly connected to the input terminals of the Unit.

6.   THE MARGINAL TESTS

The following marginal tests may be applied to the Computer or the Additional Stores when appropriate.   The tests may be followed in the diagram of the Marginal Test Unit given in Fig. E2.

6.1   + 6V, -6V, Test

In this test an MCB 21 power supply is used with the computer.

6.1.1   Set all switches to the OFF position.

6.1.2   Connect cable of the Marginal Test Unit into socket 7 of the computer.   If these tests are made on an Additional Store insert the plug into socket 12 of the Additional Store.   See Fig. A1 (Pt. 1, Chap. 1).

6.1.3   Operate meter switch S6 to the 6 VOLTS position.

6.1.4   Operate 6 VOLTS key S1 to the mid-position for Margin Inhibit.

6.1.5   Operate 6 VOLTS key to down position and adjust 6 VOLTS potentiometer RV1 for positive and negative deflection.   Failure should not occur at less than $\pm$ 10% margins at a normal ambient temperature when programs X1, X2, X3, X4, X5 and X10 are used.

6.1.6   On completion of this test return potentiometer to mid-position (corresponding to meter zero) and the 6 VOLTS key to the fully up OFF position.   A diagram of this test is given in Fig. g.

NOTE: If margin inhibit is not applied before the Margin Test, the 6 volts sensing circuit will operate and switch off the MCB 21 power supply.   This is prevented by first operating the 6 VOLTS key to the mid-position.   This routes a biasing voltage to diode D7 on the A-HJ board inhibiting the 6 volt sensing circuit.

6.2   VARIABLE SUPPLY (INHIBIT) Test

6.2.1   Repeat 6.1.1 and 6.1.2.   A diagram of this test is given in Fig. h.

6.2.2   Operate meter switch S6 to INHIBIT

6.2.3   Set INHIBIT key S2 to the ON position.
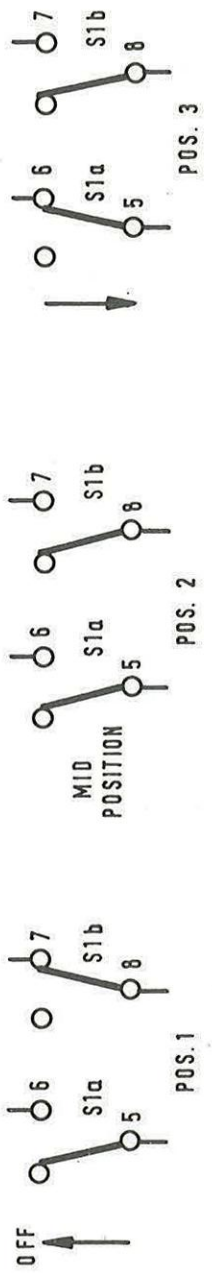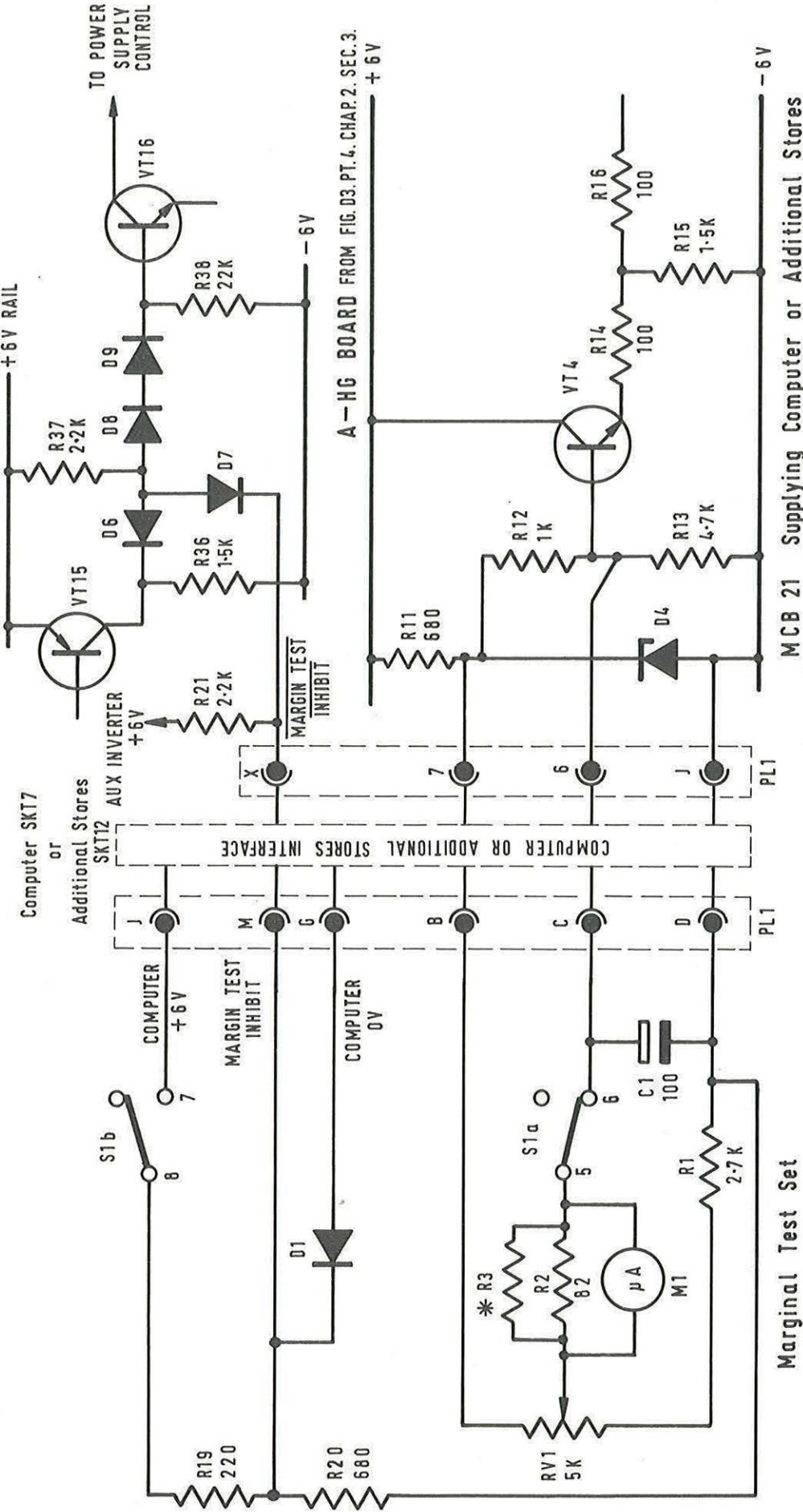
6.2.4   Adjust INHIBIT potentiometer RV2 for 15% margins of store inhibit current without failure of computer when running program X2.

6.2.5   Return potentiometer to mid-position so that the meter reads zero and switch INHIBIT key to OFF.

6.3   DRIVE CURRENT Test

6.3.1 Repeat 6.1.1 and 6.1.2.   A diagram of this test is given in Fig. i.
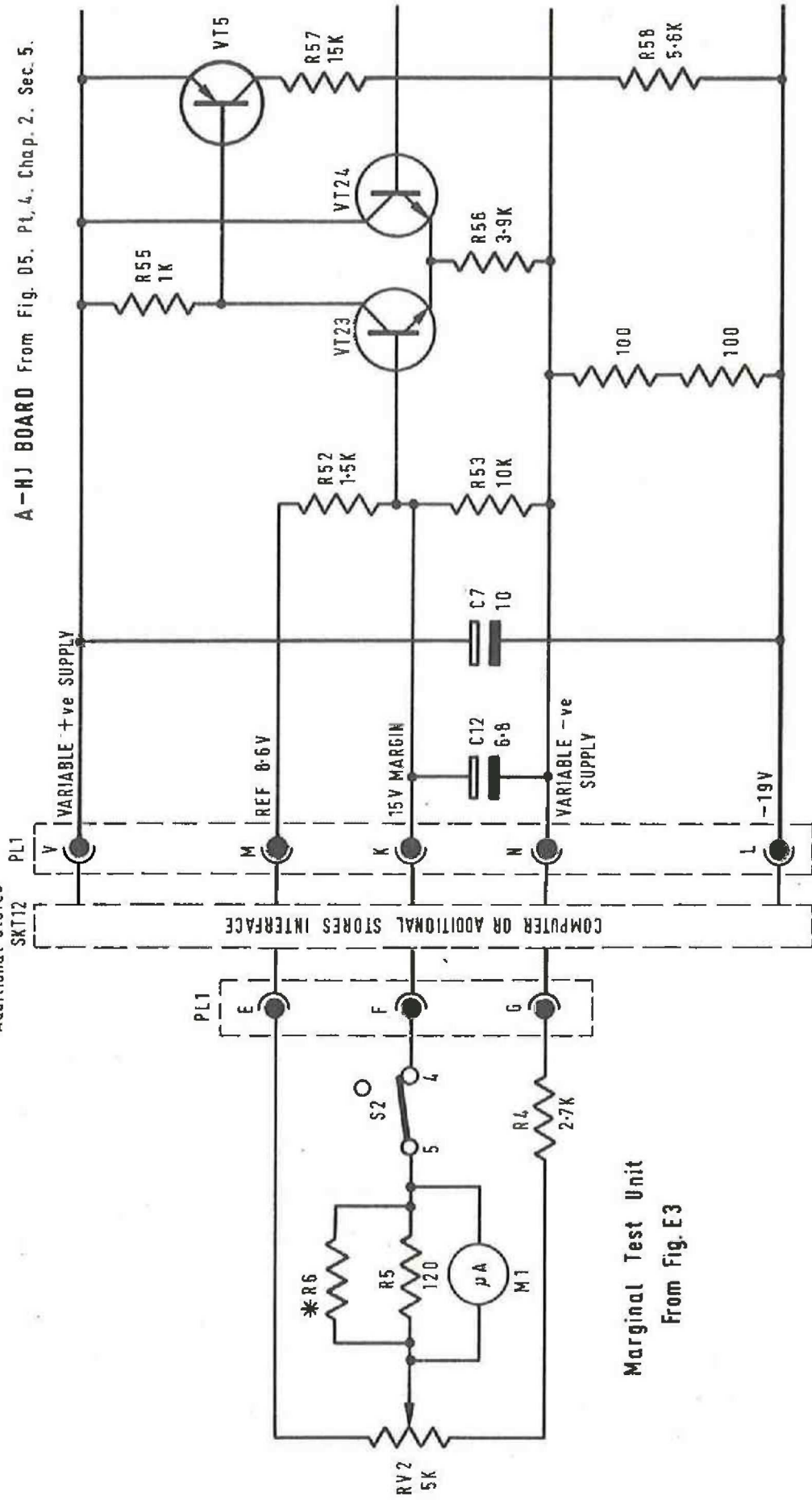
Fig. g. + 6V −6V Marginal Test

ISS. 1

NOTE: S1 is a 3 position switch used
for the + 6V −6V marginal tests
Pos. 1 No Margin Test. No Margin Inhibit.
Pos. 2 No Margin Test. Margin Inhibit.
Pos. 3 Margin Test. Margin Inhibit.

MCB 21 Supplying Computer or Additional Stores

A−HG BOARD FROM FIG. D3. PT. 4. CHAP. 2. SEC. 3.

A−HJ BOARD FROM FIG. D5. PT. 4. CHAP. 2. SEC. 5.

Marginal Test Set
From Fig. E3

Computer SKT7
or
Additional Stores
SKT12

COMPUTER OR ADDITIONAL STORES INTERFACE

* Selected on Test

Fig. h. Variable Supply (Inhibit) Marginal Test

* Selected on Test

A-EC3 Unit (Master Drivers) Computer or Additional Stores

From Fig. A33. Pt.1. Chap. 5. Sec. 6.

Fig. i. Drive Current Marginal Test

ISS. 1.

* Selected on Test

- 12 -

6.3.2   Operate meter switch S6 to DRIVE position.

6.3.3   Operate DRIVE key S3 to the ON position.

6.3.4   Adjust the DRIVE potentiometer RV3 for $\pm$ 10% margins of store drive current without failure of computer when running program X2 or X4.

6.3.5   Return potentiometer to mid-position of meter zero and the DRIVE key to the OFF position.

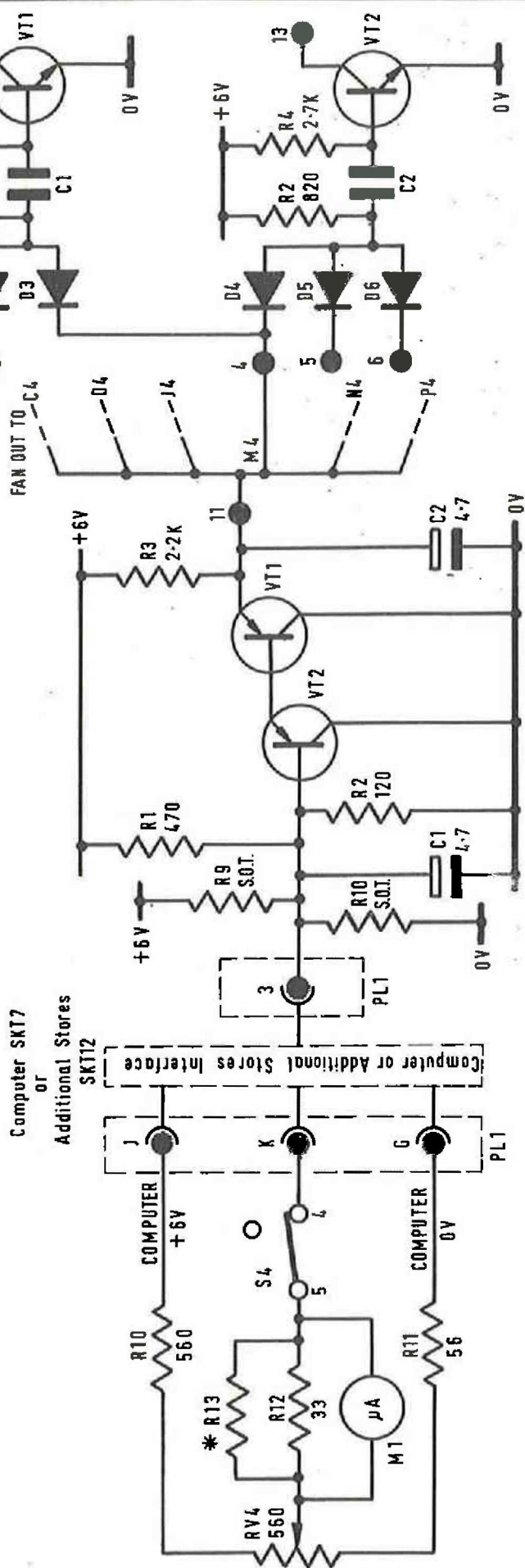6.4   MAIN TIMING LOOP Test

6.4.1   Repeat 6.1.1 and 6.1.2.   A diagram of this test is given in Fig. j.

6.4.2   Operate meter switch S6 to TIMING.

6.4.3   Set TIMING key S4 to the ON position.

6.4.4   Adjust TIMING potentiometer. RV4 for both positive and negative deflection.   Margins obtained should be greater than $\pm$ 10% before failure of the computer when running program X3.

(Issue 1)

VT1

11

+6V

R3 8·4K

R1 820

C1

D1 D2 D3

1 2

LSA 07

NOTE: LSA 07 & 08 From Fig. A6.
Pt.1. Chap. 2. Sec.5.
Main Timing Loop From Fig. A21
Pt.1. Chap. 4. Sec. 2.

VT2

13

+6V

R4 2·7K

R2 820

C2

D4 D5 D6

4 5 6

FAN OUT TO

C4

D4

J4

M4

N4

P4

+6V

R3 2·2K

11

VT1

VT2

C2 4·7

0V

Main Timing Loop
Fig. A21

R1 470

R2 120

LSA 08. 2·4V. REF.

R9 S.O.T.

+6V

C1 4·7

R10 S.O.T.

0V

3

PL1

Computer SKT7
or
Additional Stores
SKT12

Computer or Additional Stores Interface

J

K

G

PL1

COMPUTER +6V

S4

4

5

COMPUTER 0V

R10 560

R13

R12 33

μA

M1

R11 56

RV4 560

Marginal Test Unit
From Fig. E3

* Selected on Test

Fig. j. Main Timing Loop Marginal Test. (With MCB 21 or MCB 24)

ISS. 1.

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6.4.5   Return the control potentiometer to the mid-position so that the meter reads zero. Switch TIMING key to the OFF position.

NOTE: The output voltage of the 2.4V Reference Generator at pin 11 is varied by changing the voltage on pin 6 of the Reference Generator. This is given in Fig. A6, Sht 14 (Pt. 1, Chap. 2, Sec. 5.8).

The output of the 2.4V generator fans out to C4, D4, J4, M4, N4 and P4 at the Main Timing Loop. Schematic diagrams and descriptions of the pulse generators are given in Fig. A6, Sht 13 (Pt. 1, Chap. 2, Sec. 5.7), and Fig. A6, Sht 15 (Pt. 1, Chap. 2, Sec. 5.9).

The resistors R9 and R10 are chosen on Test.

6.5   PULSERS Test

6.5.1   Repeat 6.1.1 and 6.1.2. A diagram of this test is given in Fig. k.
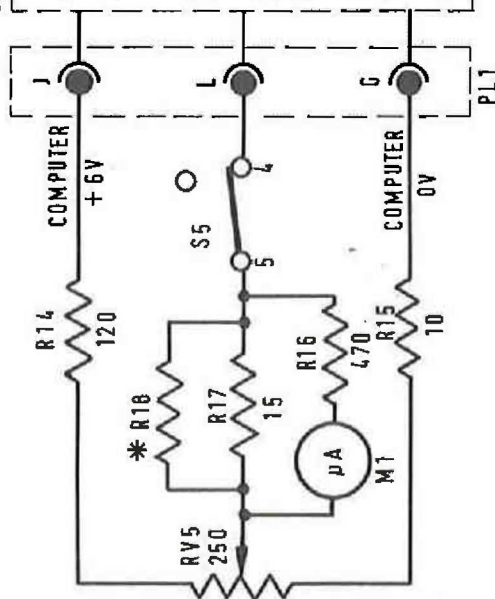
6.5.2   Operate meter switch S6 to PULSERS.

6.5.3   Operate PULSERS key S5 to the ON position.

6.5.4   Adjust PULSERS potentiometer RV5 for $\pm$ 10% in pulse width without failure when running program X3.
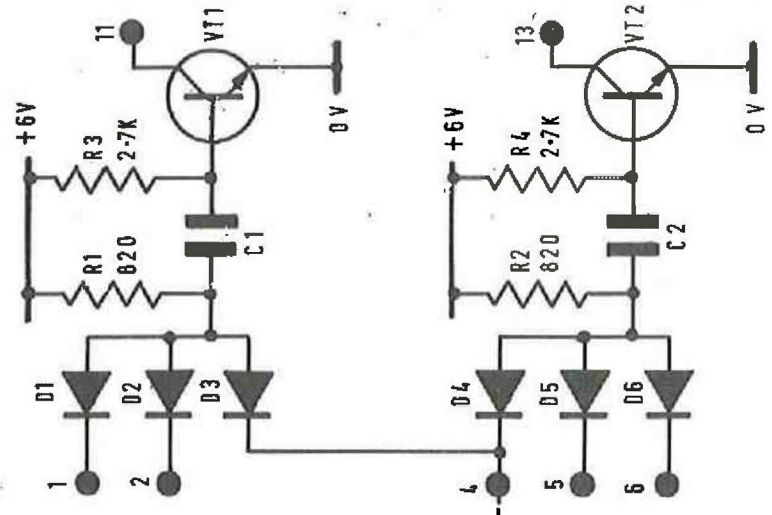
6.5.5   Return the control potentiometer to the mid-position so that the meter reads zero. Switch PULSERS key to the OFF position.

NOTE: This test is applied to all pulsers in the computer with the exception of the Main Timing Loop Fig. A21 (Pt. 1, Chap. 4, Sec. 2).

LSA 13

Pulse Generator
Fig. A15

LSA 08

Marginal Test Unit
From Fig. E3

Computer SKT7
or
Additional Stores
SKT12

Computer or Additional Stores Interface

⊗ NOTE: See Fig. A6. Chap. 2. Sec. 5 for
LSA 08,13 of Pulse Generator
Fig. A13. Pt. 1. Chap. 4.
Fig. A14. Pt. 1 Chap. 4.
Fig. A15. Pt. 1 Chap. 4.
Fig. A31 Pt. 1 Chap. 4.

ISS. 1.

Fig. k. Pulse Generator Marginal Test (MCB 24).

* Selected on Test

MCS 920B COMPUTER TECHNICAL MANUAL

CATALOGUE NO. MCB 143

PART 5: OPERATIONAL/TEST EQUIPMENT

CHAPTER 5: START ADDRESS PLUG, MCB 42

CHAPTER 5

START ADDRESS PLUG, MCB 42

CONTENTS

LIST OF FIGURES

(v)

CHAPTER 5

START ADDRESS PLUG (MCB 42)

1.   GENERAL

The Start Address Plug may be used in place of a Control Unit when the computer is to be used on a fixed program. The effect of the plug is to cause the computer automatically to enter the program retained in the store as soon as power is applied.

NOTE: The plug can be used only when a program has been placed in the store via a Control Unit and Tape reader or a Program Loading Unit.

With power removed from the computer, the Start Address Plug is placed in computer SKT 11 (which is one of two sockets which otherwise connect to the Control Unit), Fig. A1 refers.

2.   EFFECTS

The effects of the plug are as follows:

i)   The computer is switched on automatically as soon as power is applied to the computer power supply unit.   (MCB 21 or equivalent).
NOTE: The Start Address Plug cannot be used with power supply MCB 24).

ii)   After switch-on, the computer assumes the Reset state and then performs an automatic jump to location 8177; this location should contain a jump to the start of the program. If the (internal) store is below its operating temperature, the jump is delayed until the

- 1 -   (Issue 1)

temperature is attained (the core stack heaters
are automatically switched on in these cir-
cumstances).

iii)   Peripheral interrupt signals are enabled but
manual interrupts are not possible.

A simplified diagram showing the links made by the Start Address
Plug when connected to computer SKT 11 is given by Fig. E3.